IN THE CLAIMS:

Please note that all of the claims that remain pending and under consideration in the above-referenced application are shown below, in clean form, for clarity. Also attached is a marked-up version of each amended claim to show the changes that have been made thereto.

Please cancel claims 4, 42, and 56 through 72 without prejudice or disclaimer.

Please enter the claims as follows:

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1. (Amended) A chip-scale package, comprising:

a semiconductor device including an active surface; and

a substrate comprising a semiconductor material disposed adjacent said active surface and including:

at least one electrically conductive via extending at least partially therethrough and being in communication with a corresponding bond pad of said semiconductor device; and

at least one conductive trace carried on a surface of said substrate which is opposite from another surface of said substrate that is adjacent to said semiconductor device.

2. (Amended) The chip-scale package of claim 1, further comprising an electrically conductive bump protruding from said substrate opposite said semiconductor device and in communication with said at least one electrically conductive via.

3. (Twice amended) The chip-scale package of claim 1, wherein said substrate comprises at least another electrically conductive via that extends substantially directly therethrough.

5. (Amended) The chip-scale package of claim 1, wherein a substrate of said semiconductor device and said substrate comprising semiconductor material comprise the same type of semiconductor material.

6. (Amended) The chip-scale package of claim 1, wherein a substrate of said semiconductor device and said substrate comprising semiconductor material comprise materials having substantially the same coefficients of thermal expansion.

7. The chip-scale package of claim 1, wherein a substrate of said semiconductor device comprises silicon.

8. (Amended) The chip-scale package of claim 1, wherein said semiconductor material comprises silicon.

9. (Amended) The chip-scale package of claim 1, wherein a first thickness of said semiconductor device and a second thickness of said substrate are substantially the same.

10. (Amended) The chip-scale package of claim 1, wherein a first thickness of said semiconductor device is greater than a second thickness of said substrate.

11. (Amended) The chip-scale package of claim 1, wherein said another surface of said substrate is at least partially coated with an insulative material.

12. The chip-scale package of claim 11, wherein said insulative material comprises a layer extending substantially over said surface.

13. The chip-scale package of claim 11, wherein said insulative material comprises an oxide.

14. The chip-scale package of claim 11, wherein said insulative material comprises silicon oxide.

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15. (Amended) The chip-scale package of claim 1, further comprising an intermediate layer disposed between said semiconductor device and said substrate.

16. The chip-scale package of claim 15, wherein said intermediate layer comprises an adhesive material.

17. The chip-scale package of claim 15, wherein said intermediate layer comprises polyimide.

18. The chip-scale package of claim 15, wherein said at least one electrically conductive via and said corresponding bond pad communicate through said intermediate layer.

19. The chip-scale package of claim 1, wherein conductive material of said at least one electrically conductive via is bonded to said corresponding bond pad.

20. The chip-scale package of claim 1, wherein a contact between said at least one electrically conductive via and said corresponding bond pad comprises a diffusion region comprising a bond pad material and a via material.

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21. (Amended) A chip-scale package, comprising:

a substrate comprising semiconductor material and including:

a first surface with contact areas arranged correspondingly to an arrangement of bond pads on an active surface of a semiconductor device of the chip-scale package;

conductive vias extending therethrough and corresponding to said contact areas; and

a second surface carrying at least one conductive trace extending laterally from a conductive via of said conductive vias; and

said semiconductor device invertedly disposed adjacent said substrate so that bond pads of said semiconductor device communicate through corresponding conductive vias of said substrate.

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22. (Amended) The chip-scale package of claim 21, wherein said bond pads contact said corresponding conductive vias.

23. (Amended) The chip-scale package of claim 22, further comprising diffusion regions between said bond pads and said corresponding conductive vias.

24. (Amended) The chip-scale package of claim 23, wherein each of said diffusion regions comprises a bond pad material and a via material.

25. (Amended) The chip-scale package of claim 24, wherein said diffusion regions at least partially secure said semiconductor device to said substrate.

26. (Amended) The chip-scale package of claim 21, further comprising an intermediate layer disposed between said substrate and said semiconductor device.

27. (Amended) The chip-scale package of claim 26, wherein said bond pads and said corresponding vias contact each other through said intermediate layer.

28. (Amended) The chip-scale package of claim 26, wherein said intermediate layer comprises a material which adheres said semiconductor device to said substrate.

29. The chip-scale package of claim 26, wherein said intermediate layer comprises a polyimide.

30. (Amended) The chip-scale package of claim 21, further comprising at least one conductive bump in communication with at least one conductive via of said corresponding conductive vias and protruding from said substrate opposite from said semiconductor device.

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31. (Amended) The chip-scale package of claim 30, wherein said at least one conductive bump comprises solder.

32. (Amended) The chip-scale package of claim 21, wherein said substrate comprising semiconductor material and a substrate of said semiconductor device comprise the same material.

33. (Amended) The chip-scale package of claim 21, wherein said substrate comprises silicon.

34. The chip-scale package of claim 21, wherein a substrate of said semiconductor device comprises silicon.

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35. (Amended) The chip-scale package of claim 21, wherein a first thickness of said substrate and a second thickness of said semiconductor device are substantially equal.

36. (Amended) The chip-scale package of claim 21, wherein a first thickness of said substrate is less than a second thickness of said semiconductor device.

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37. (Amended) The chip-scale package of claim 21, further comprising an insulative material disposed on at least a portion of said second surface of said substrate.

38. (Amended) The chip-scale package of claim 37, wherein at least one conductive via of said corresponding conductive vias is exposed through said insulative material.

39. The chip-scale package of claim 37, wherein said insulative material comprises an oxide.

40. The chip-scale package of claim 37, wherein said insulative material comprises silicon oxide.

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41. (Amended) The chip-scale package of claim 37, wherein said insulative material comprises an insulative layer disposed substantially over said second surface.

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43. (Twice amended) A flip-chip carrier, comprising a substrate comprising semiconductor material and including:

at least one via formed therethrough and having a first end located proximate a first surface of said substrate and positioned to substantially align with a corresponding bond pad of a semiconductor device to be assembled with said substrate; and

at least one conductive trace laterally extending from a second end of said at least one via and carried by a second surface of said substrate.

44. The flip-chip carrier of claim 43, wherein said at least one via comprises an electrically conductive material.

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45. (Amended) The flip-chip carrier of claim 43, further comprising an insulative material disposed on at least a portion of at least one surface of said substrate.

46. The flip-chip carrier of claim 45, wherein said insulative material comprises an oxide.

47. The flip-chip carrier of claim 45, wherein said insulative material comprises silicon oxide.

48. The flip-chip carrier of claim 45, wherein said insulative material comprises an insulative layer disposed substantially over said at least one surface.

49. The flip-chip carrier of claim 45, wherein said at least one via is exposed through said insulative material.

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50. (Amended) The flip-chip carrier of claim 43, wherein said substrate comprises silicon.

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51. (Twice amended) The flip-chip carrier of claim 43, further comprising a conductive bump disposed adjacent an end of said at least one conductive trace located opposite from said second end of said at least one via.

52. The flip-chip carrier of claim 51, wherein said conductive bump comprises solder.

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53. (Amended) The flip-chip carrier of claim 43, further comprising an adhesive layer disposed adjacent said first surface of said substrate.

54. The flip-chip carrier of claim 53, wherein said adhesive layer comprises a polyimide.

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55. (Amended) The flip-chip carrier of claim 53, wherein said first end of said at least one via extends through said adhesive layer.